CLAIMS

1. A transistor comprising a spin injector injecting spin-polarized hot carriers by a spin filter effect, and a spin analyzer selecting the injected spin-polarized hot carriers by the spin filter effect.

2. The transistor according to claim 1, wherein said spin injector has a first ferromagnetic barrier layer capable of tunneling carriers by applying a voltage at both ends, a first nonmagnetic electrode layer joined to one end surface of said first ferromagnetic barrier layer, and a second nonmagnetic electrode layer joined to the other end surface of said first ferromagnetic barrier layer.

3. The transistor according to claim 1 or 2, wherein said spin analyzer has a second ferromagnetic barrier layer, said second nonmagnetic electrode layer joined to one end surface of the second ferromagnetic barrier layer, and a third nonmagnetic electrode layer joined to the other end surface of said second ferromagnetic barrier layer, and shares said second nonmagnetic electrode layer with said spin injector.

4. The transistor according to claim 2 or 3, wherein said first and second ferromagnetic barrier layers include a ferromagnetic semiconductor or a ferromagnetic insulator.

5. The transistor according to any one of claims 1 to 4, wherein the thickness of said second nonmagnetic electrode layer is below the mean free path of spin-polarized hot carriers of said second nonmagnetic electrode layer.

6. The transistor according to any one of claims 1 to 5, wherein according to the spin filter effect of said spin injector, in the tunnel effect of the carriers in said first ferromagnetic barrier layer produced by applying a voltage to said first nonmagnetic electrode layer and said second nonmagnetic electrode layer, large is the tunnel probability of the carriers having the direction of the spin parallel to the spin band at the band edge of said first ferromagnetic barrier layer of the carriers existing in said first nonmagnetic electrode layer, and small is the tunnel probability of the carriers having the direction of the spin anti-parallel thereto.

7. The transistor according to any one of claims 1 to 6, wherein according to the spin filter effect of said spin analyzer, when the direction of the spin of spin-polarized hot carriers injected from said spin injector is parallel to the direction of the spin of the spin band at the band edge of said second ferromagnetic barrier layer, said spin-polarized hot carriers are conducted through the spin band at the band edge of said second ferromagnetic barrier layer to reach said third nonmagnetic electrode layer, and when the direction of the spin of said spin-polarized hot carriers is anti-parallel to the direction of the spin of the spin band at the band edge of said second ferromagnetic barrier layer, said spin-polarized hot carriers cannot reach said third nonmagnetic electrode layer.

8. The transistor according to any one of claims 1 to 7, wherein a first voltage is applied by a first power source between said first nonmagnetic electrode layer and said second nonmagnetic electrode layer, a second voltage is applied by a second power source between said second nonmagnetic electrode layer and said third nonmagnetic

electrode layer or between said first nonmagnetic electrode layer and said third nonmagnetic electrode layer, and according to the relative directions of magnetization of said first ferromagnetic barrier layer and said second ferromagnetic barrier layer, spin-polarized hot carriers injected from said first nonmagnetic electrode layer into said second nonmagnetic electrode layer are switched to either an electric current flowing via said second ferromagnetic barrier layer and said second power source or an electric current flowing via said second nonmagnetic electrode layer and said first power source.

9. The transistor according to claim 8, wherein said first voltage is applied so that the energy of the injected spin-polarized hot carriers is larger than the energy of the spin band edge of said second ferromagnetic barrier layer and is smaller than the energy in which a spin split width is added to the energy of the spin band edge.

10. The transistor according to claim 9, wherein a magnetic field is applied to invert any one of the directions of magnetization of said first ferromagnetic barrier layer and said second ferromagnetic barrier layer.

11. A memory circuit wherein the transistor according to any one of claims 1 to 10 is a memory cell.

12. The memory circuit according to claim 11, wherein the second nonmagnetic electrode layer of said transistor is connected to a word line, the third nonmagnetic electrode layer of said transistor is connected to a bit line, said bit line is connected via a load to a power

source, and the first nonmagnetic electrode layer of said transistor is grounded.

13. A storage device comprising:

a transistor (hereinafter, called a "spin transistor") including ferromagnetic substances and having an output characteristic depending on the direction of the spin of carriers;

information rewriting means rewriting information in said spin transistor by changing the magnetization state of said ferromagnetic substances; and

information reading means reading information stored in said spin transistor as the magnetization state from said output characteristic.

14. The storage device according to claim 13,

wherein said spin transistor has at least one ferromagnetic substance (hereinafter, called a "free layer") capable of independently controlling the direction of magnetization and at least one ferromagnetic substance (hereinafter, called a "pin layer") not changing the direction of magnetization, and holds any one of two stored states of a first state in which said free layer and said pin layer have the same direction of magnetization and a second state having different directions of magnetization.

15. A storage device wherein one spin transistor according to claim 14 is used to store information according to the relative directions of magnetization of said pin layer and said free layer for detecting the information stored in said transistor based on an output characteristic

of said spin transistor depending on the relative directions of magnetization of said pin layer and said free layer.

16. The storage device according to claim 14 or 15,

wherein said spin transistor has a first electrode structure injecting spin-polarized carriers, a second electrode structure receiving said spin-polarized carriers, and a third electrode structure controlling the quantity of the spin-polarized carriers conducted from said first electrode structure to said second electrode structure, and said pin layer and said free layer are included in any one of said first to third electrode structures.

17. A storage device comprising:

one spin transistor according to claim 16;

a first wire grounding said first electrode structure;

a second wire connected to said second electrode structure; and

a third wire connected to said third electrode structure.

18. A storage device comprising:

one spin transistor according to claim 16;

a first wire grounding said first electrode structure;

a second wire connected to said second electrode structure;

a third wire connected to said third electrode structure;

an output terminal formed at one end of said second wire; and

a fourth wire branched from said second wire to be connected via a load to a power source.

19. The storage device according to claim 17 or 18, further comprising a first another wire and a second another wire crossing on said spin transistor to be electrically insulated from each other.

20. The storage device according to claim 19, wherein in place of said first another wire and said second another wire or any one of said first another wire and said second another wire, said second wire and said third wire are used or any one of said second wire and said third wire is used.

21. The storage device according to claim 19 or 20, wherein a magnetic field induced by flowing electric currents to said first another wire and said second another wire or said second wire and said third wire inverts the magnetization of said free layer to change the relative magnetization state of said pin layer and said free layer for rewriting information.

22. The storage device according to claim 17 or 18, wherein information is read based on an output characteristic of said spin transistor when applying a first bias to said third wire and a second bias between said first wire and said second wire.

23. The storage device according to any one of claims 18 to 22, wherein when applying a first bias to said third wire, information is read by an output voltage obtained based on the voltage drop of said load produced between said power source and said first wire and said load by an electric current via said spin transistor.

24. A memory circuit comprising:

one spin transistor according to claim 16 arrayed in matrix;

a first wire grounding each of said first electrode structures;

a plurality of word lines sharably connecting said third electrode structures of said spin transistors arrayed in the column direction; and

a plurality of bit lines sharably connecting said second electrode structures of said spin transistors arrayed in the row direction.

25. A memory circuit comprising:

a spin transistor according to claim 16 arrayed in matrix;

a first wire grounding each of said first electrode structures;

a plurality of word lines sharably connecting said third electrode structures of said spin transistors arrayed in the column direction;

a plurality of bit lines sharably connecting said second electrode structures of said spin transistors arrayed in the row direction;

an output terminal formed at one end of said bit line; and

a second wire branched from said bit line to be connected via a load to a power source.

26. The memory circuit according to claim 24 or 25, further comprising a first another wire and a second another wire crossing on said transistor to be electrically insulated from each other.

27. The memory circuit according to claim 26, wherein in place of said first another wire and said second another wire or any one of said first

another wire and said second another wire, said word line and said bit line are used or any one of said word line and said bit line is used.

28. The memory circuit according to claim 26 or 27, wherein a magnetic field induced by flowing electric currents to said first another wire and said second another wire or said word line and said bit line inverts the magnetization of said free layer to change the relative magnetization state of said free layer and said pin layer for rewriting information.

29. The memory circuit according to claim 24 or 25, wherein information is read based on an output characteristic of said spin transistor when applying a first bias to said word line and a second bias between said first wire and said bit line.

30. The memory circuit according to any one of claims 25 to 27, wherein when applying a first bias to said word line, information is read by an output voltage obtained based on the voltage drop of said load produced between said power source and said first wire and said load by an electric current via said spin transistor.

31. A storage device comprising:

a first and second spin transistors according to claim 16;

a first wire grounding a first electrode structure shared between said first and second spin transistors;

a second and third wires connecting a second electrode structure of said first spin transistor and a second electrode structure of said second spin transistor, respectively; and

a fourth wire connecting a third electrode structure of said first spin transistor and a third electrode structure of said second spin transistor.

32. A memory circuit comprising:

a plurality of spin transistors according to claim 16 arrayed in matrix;

a first wire sharing and grounding said first electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction and in the row of a plurality of second spin transistors arrayed in the row direction adjacent to the row of said first spin transistors in the column direction;

a first bit line sharably connecting said second electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction, and a second bit line sharably connecting said second electrode structures in the row of second spin transistors adjacent to the row of said first spin transistors in the column direction; and

a word line sharably connecting third electrode structures, of said plurality of spin transistors, in the column of a plurality of spin transistors arrayed in the column direction.

33. A memory circuit comprising:

a plurality of spin transistors according to claim 16 arrayed in matrix;

a plurality of first wires sharing and grounding said first electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction and

in the row of a plurality of second spin transistors arrayed in the row direction adjacent to the row of said first spin transistors in the column direction, one first wire being provided every two rows;

a plurality of first bit lines sharably connecting said second electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction, one first bit line being provided every two rows of said spin transistors, and a plurality of second bit lines sharably connecting said second electrode structures in the row of second spin transistors adjacent to the row of said first spin transistors in the column direction, one second bit line being provided every two rows of said spin transistors; and

a plurality of word lines sharably connecting third electrode structures, of said plurality of spin transistors, in the column of a plurality of spin transistors arrayed in the column direction.

34. The storage device according to claim 20, wherein a magnetic field induced by flowing electric currents to said second wire or said third wire with which any one of said first another wire and said second another wire is replaced and said first another wire or said second another wire which is not replaced with these inverts the magnetization of said free layer to change the relative magnetization state of said pin layer and said free layer for rewriting information.

35. The memory circuit according to claim 27, wherein a magnetic field induced by flowing electric currents to said word line or said bit line with which any one of said first another wire and said second another wire is replaced and said first another wire or said second another wire which is not replaced with these changes the relative

magnetization state of said free layer and said pin layer for rewriting information.